ADM-VB630-RTM
User Manual

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1 Introduction

The **ADM-VB630-RTM ("RTM")** shall be a commercial grade 3U RTM for lab testing and development use of the ADM-VB630 ("VB630"). The RTM will allow access to all IO made available by the ADM-VB630 on the VPX backplane.

1.1 Key Features

Key Features

- 3U VPX form factor
- Allow access to all IO made available by the VB630 on the VPX backplane.
- 2x QSFP connectors for SpaceFibre or other protocol use.
- HSDP debug connector access to the VB630.
- 1x Spacewire Connector and 1x Spacewire header.
- 2x CAN Bus headers.
- 2x UART : 1x USB and 1x header.
- Gigabit Ethernet RJ45.
- GIPO / MIO breakout from the VB630.

1.2 References & Specifications

ANSI/VITA 46.0	*VPX Baseline Standard*, October 2007, VITA, ISBN 1-885731-44-2
ANSI/VITA 46.4	*PCI Express® on the VPX Fabric Connector*, July 2010, VITA, Draft 0.15
ANSI/VITA 46.6	*Gigabit Ethernet Control Plane on VPX*, September 2010, VITA, Draft 0.7
ANSI/VITA 46.11	*System Management on VPX*, June 2015, VITA, ISBN 1-885731-84-1
ANSI/VITA 65	*OpenVPX™ System Specification*, June 2010, VITA, ISBN 1-885731-58-2
ANSI/VITA 67.0	*Coaxial Interconnect on VPX – Base Standard*, April 2019, VITA, ISBN 978-1-948739-09-2
ANSI/VITA 67.3	*Coaxial Interconnect on VPX,Spring-Loaded Contact on Backplane*, December 2017, VITA, ISBN 978-1-948739-00-9
ANSI/VITA 78.0	*SpaceVPX System*, April 2015, VITA, ISBN 1-885731-83-3
ANSI/VITA 48.2	*Mechanical Specifications for Microcomputers Using REDI Conduction Cooling Applied to VITA VPX*, July 2010, VITA, ISBN 1-885731-60-4
SpaceWire Standard	*SpaceWire Standard*, 23 November 2015, ECSS

Table 1 : References

2 Installation

2.1 Software Installation

Please refer to the ADM-VB630 area on the Alpha-Data support site for access to system monitoring utilities, documentation and FPGA reference designs.

2.2 Hardware Installation

2.2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

3 Functional Description

3.1 Block Diagram

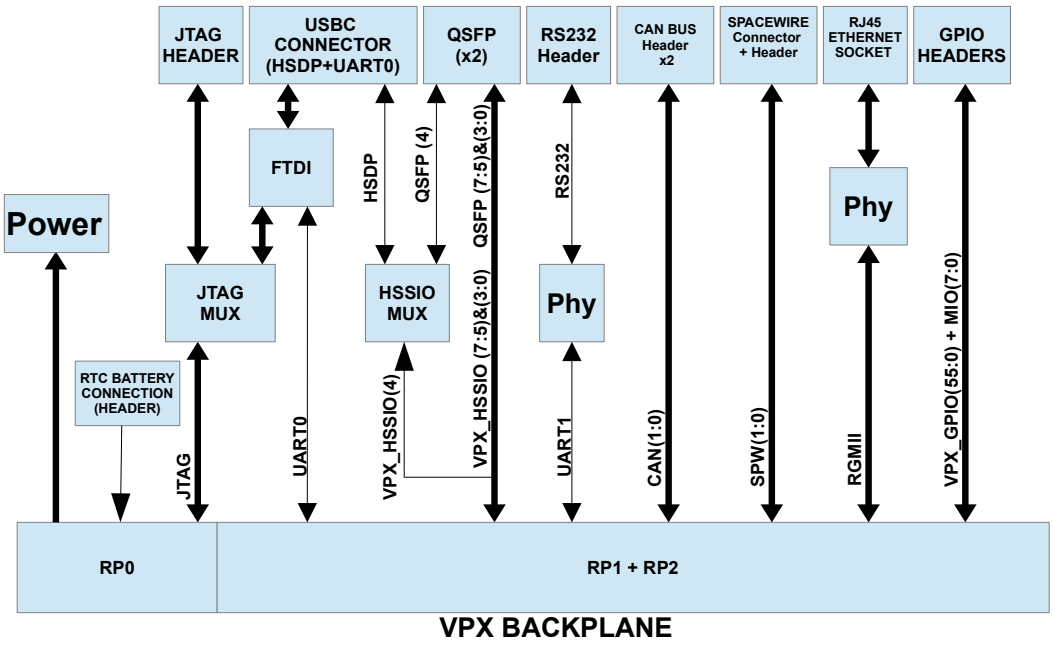

Figure 1 : ADM-VB630-RTM Block Diagram

3.2 Assembly Drawing

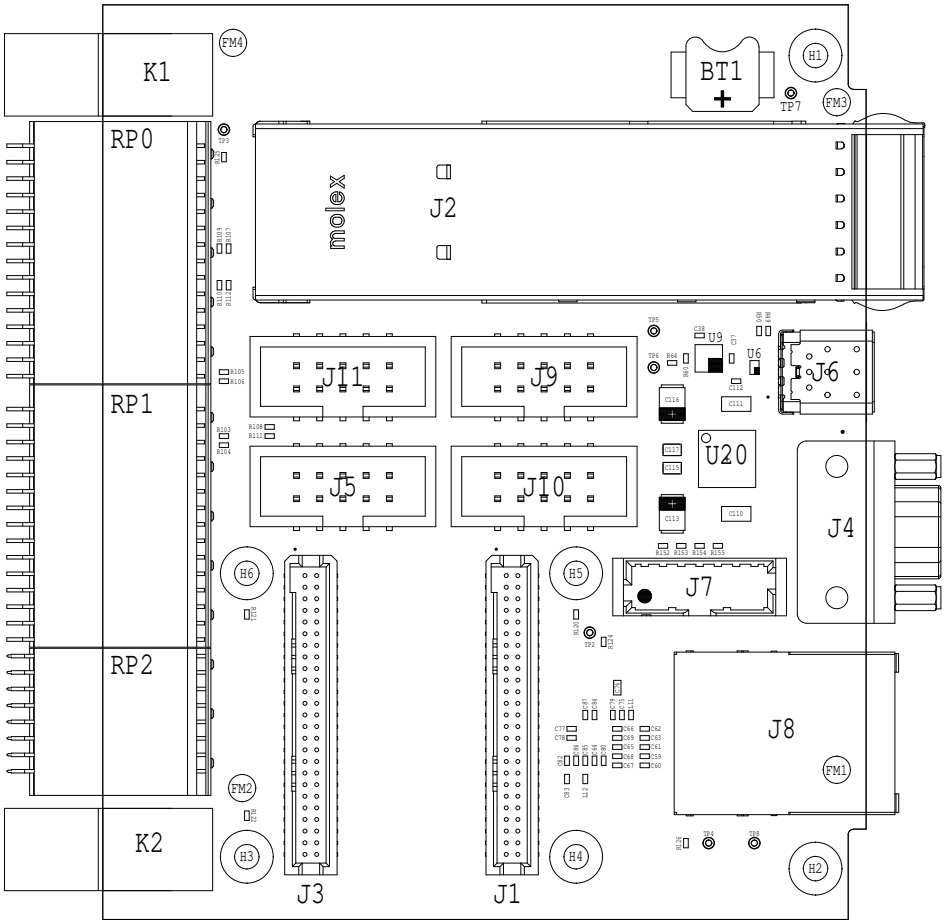

Figure 2 : ADM-VB630-RTM Top View

3.3 Switch Definitions

There are two sets of eight DIP switches placed on the bottom of the board. Their functions are described below.

Note:
All switches are OFF by default. All SW2 switches and switches SW1.3,4,5,8 must be in the OFF position for normal operation.

Switch Ref.	Function	ON State	Off State
SW1-1	HSSIO mux	QSFP Port	USBC port (HSDP)
SW1-2	QSFP I2C Comms	Enabled	Disabled
SW1-3	VPX Test CLK Gen	Enabled	Disabled
SW1-4	PSU_ON	Low	High
SW1-5	NVMRO	Low	High
SW1-6	USB UART	Disabled	Enabled
SW1-7	MSKRST_L	Low	High
SW1-8	VPX_SYSRESET_L	Low	High

Table 2 : Control Switches (SW1)

Switch Ref.	Function	ON State	Off State
SW2-1	VPX_GAP	Low	Tri-state
SW2-2	VPX_GA0	Low	Tri-state
SW2-3	VPX_GA1	Low	Tri-state
SW2-4	VPX_GA2	Low	Tri-state
SW2-5	VPX_GA3	Low	Tri-state
SW2-6	VPX_GA4	Low	Tri-state
SW2-7	SYSCON_L	Low	Tri-state
SW2-8	GDISC1	Low	Tri-state

Table 3 : VPX Test Switches (SW2)

3.4 Connector Definitions

The description of the connectors on the board status shown below:

Comp. Ref.	Function
J1+J3	GPIO Headers
J2	QSFP x2 Connectors
J4	Spacewire Connector
J5	Spacewire Header
J6	USBC Connector
J7	AMD Programming cable Connector
J8	Ethernet
J9+J10	CANBUS Headers
BT1	RTC Battery Holder
J11	RS232 Serial Port Header

Table 4 : Connector Definitions

3.5 LED Definitions

The position and description of the user LEDs is shown in LED Locations:

The user LEDs are active low, and will illuminate when the signal = logic low.

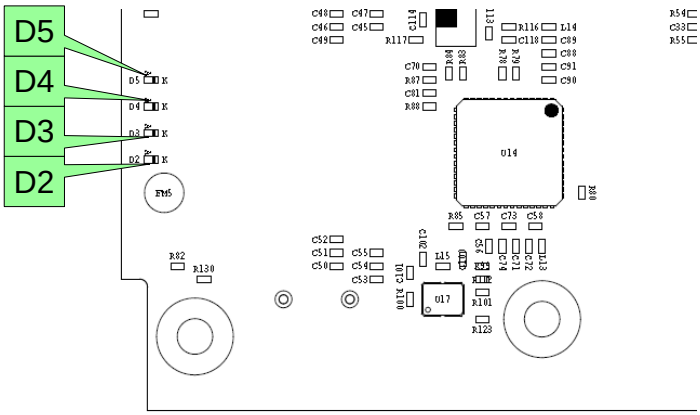

Figure 3 : LED Locations

Comp. Ref.	Signal Name	FPGA pin
D2(Green)	GPIO55	J22
D3(Green)	GPIO54	J21
D4(Green)	GPIO53	L22
D5(Green)	GPIO52	K21

Table 5 : LED Definitions

3.6 JTAG Interface

3.6.1 USB Programming

A JTAG boundary scan chain is connected to either an on-board USB to JTAG converter via connector J6, or 14-pin JTAG header J7. The on-board USB to JTAG converter is enabled whenever a USB connection is made.

3.6.2 Standard Header

As stated in the previous section, the JTAG boundary scan chain can also be accessed via a standard header (J7).

This allows the connection of the AMD JTAG cable for FPGA debug and Flash programming via the AMD toolchain.

3.6.3 JTAG Voltages

The Vcc supply provided to the JTAG cable on the config header is +3.3V and is protected by a poly fuse rated at 350mA.

3.7 Ethernet Phy Interface Signals

The reset_n pin of the Ethernet Phy is connected directly to the VPX system reset.

The Ethernet Phy MDIO BUS interface should be configured as shown in the table below:

Signal Name	FPGA Pin
MDC	PSMIO50 (AB10)
MDIO	PSMIO51 (AA10)

Table 6 : MDIO pins

3.8 QSFP Connectors

Connector	Ref Des	FPGA Bank
0	J2A	MGT Quad 103
1	J2B	MGT Quad 104

Table 7 : QSFP Connectors

3.9 CAN BUS 0 Header

The CAN BUS 0 interface should be configured to PSMIO14/PSMIO15 (pins T4/T5) on the PS side of the FPGA on the ADM-VB630 board.

Pin	Signal Name
1	-
2	open (can be signal ground via resistor)
3	CAN0_L
4	CAN0_H

Table 8 : Header J9 (continued on next page)

Pin	Signal Name
5	open (can be signal ground via resistor)
6	-
7	-
8	-
9	open (can be chassis ground via resistor)
10	-

Table 8 : Header J9

3.10 CAN BUS 1 Header

The CAN BUS 1 interface should be configured to PSMIO24/PSMIO25 (pins Y8/Y9) on the PS side of the FPGA on the ADM-VB630 board.

Pin	Signal Name
1	-
2	open (can be signal ground via resistor)
3	CAN1_L
4	CAN1_H
5	open (can be signal ground via resistor)
6	-
7	-
8	-
9	open (can be chassis ground via resistor)
10	-

Table 9 : Header J10

3.11 RS232 Header

Pin	Signal Name	FPGA Pin
1	-	-
2	-	-
3	TXD1	PSMIO12 (W4)
4	-	-
5	RXD1	PSMIO13 (V4)
6	-	-

Table 10 : Header J11 (continued on next page)

Pin	Signal Name	FPGA Pin
7	-	-
8	-	-
9	GND	-
10	-	-

Table 10 : Header J11

3.12 Spacewire Connector

Pin	Signal Name
1	SPW01_DIN_P
2	SPW01_SIN_P
3	GND
3	SPW01_SOUT_N
4	SPW01_DOUT_N
6	SPW01_DIN_N
7	SPW01_SIN_N
8	SPW01_SOUT_P
9	SPW01_DOUT_P

Table 11 : Header J4

3.13 Spacewire Header

Pin	Signal Name
1	SPW02_DIN_P
2	SPW02_DIN_N
3	SPW02_SIN_P
4	SPW02_SIN_N
5	GND
6	SPW02_SOUT_P
7	SPW02_SOUT_N
8	SPW02_DOUT_P
9	SPW02_SOUT_N
10	Chassis GND

Table 12 : Header J5

3.14 GPIO Headers

Signal	Pin	ACAP		ACAP	Pin	Signal
3V3	J1.1	-	|	-	J3.1	3V3
3V3	J1.2	-	|	-	J3.2	3V3
-	J1.3	-	|	-	J3.3	-
-	J1.4	-	|	-	J3.4	-
-	J1.5	-	|	-	J3.5	-
-	J1.6	-	|	-	J3.6	-
-	J1.7	-	|	-	J3.7	-
-	J1.8	-	|	-	J3.8	-
GPIO(0)	J1.9	J27	|	C23	J3.9	GPIO(28)
GPIO(1)	J1.10	H28	|	B23	J3.10	GPIO(29)
GPIO(2)	J1.11	H27	|	A23	J3.11	GPIO(30)
GPIO(3)	J1.12	G28	|	A24	J3.12	GPIO(31)
GND	J1.13	-	|	-	J3.13	GND
GND	J1.14	-	|	-	J3.14	GND
GPIO(4)	J1.15	G27	|	G21	J3.15	GPIO(32)
GPIO(5)	J1.16	F28	|	H22	J3.16	GPIO(33)
GPIO(6)	J1.17	E27	|	E20	J3.17	GPIO(34)
GPIO(7)	J1.18	E28	|	F21	J3.18	GPIO(35)
GPIO(8)	J1.19	C27	|	D20	J3.19	GPIO(36)
GPIO(9)	J1.20	B28	|	D21	J3.20	GPIO(37)
GPIO(10)	J1.21	H25	|	B20	J3.21	GPIO(38)
GPIO(11)	J1.22	J26	|	C21	J3.22	GPIO(39)
GPIO(12)	J1.23	G25	|	C22	J3.23	GPIO(40)
GPIO(13)	J1.24	G26	|	B22	J3.24	GPIO(41)
GND	J1.25	-	|	-	J3.25	GND
GND	J1.26	-	|	-	J3.26	GND
GPIO(14)	J1.27	F26	|	F23	J3.27	GPIO(42)
GPIO(15)	J1.28	E26	|	F24	J3.28	GPIO(43)
GPIO(16)	J1.29	C25	|	E24	J3.29	GPIO(44)
GPIO(17)	J1.30	B25	|	F25	J3.30	GPIO(45)
GPIO(18)	J1.31	A25	|	D25	J3.31	GPIO(46)
GPIO(19)	J1.32	A26	|	D26	J3.32	GPIO(47)
GPIO(20)	J1.33	B26	|	R21	J3.33	GPIO(48)
GPIO(21)	J1.34	B27	|	P22	J3.34	GPIO(49)
GPIO(22)	J1.35	H23	|	N21	J3.35	GPIO(50)
GPIO(23)	J1.36	H24	|	M21	J3.36	GPIO(51)

Table 13 : Headers J1 and J3 (continued on next page)

Signal	Pin	ACAP		ACAP	Pin	Signal
GPIO(24)	J1.37	E22	|	K21	J3.37	GPIO(52)
GPIO(25)	J1.38	E23	|	L22	J3.38	GPIO(53)
GPIO(26)	J1.39	D24	|	J21	J3.39	GPIO(54)
GPIO(27)	J1.40	C24	|	J22	J3.40	GPIO(55)
-	J1.41	-	|	-	J3.41	-
-	J1.42	-	|	-	J3.42	-
-	J1.43	-	|	-	J3.43	-
-	J1.44	-	|	-	J3.44	-
MIO(16)	J1.45	AF3	|	AF4	J2.45	MIO(20)
MIO(17)	J1.46	AG3	|	AE4	J2.46	MIO(21)
MIO(18)	J1.47	AH3	|	AD4	J2.47	MIO(22)
MIO(19)	J1.48	AH4	|	AC4	J2.48	MIO(23)
GND	J1.49	-	|	-	J3.49	GND
GND	J1.50	-	|	-	J3.50	GND

Table 13 : Headers J1 and J3

Revision History

Date	Revision	Nature of Change
12 February 2025	1.0	Initial Release

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